UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,210	08/20/2003	Jude A. Rivers	YOR920030249US1	5458

			EXAMINER
33233	7590	06/16/2006	ELMORE, REBA I

LAW OFFICE OF CHARLES W. PETERSON, JR. Yorktown
11703 BOWMAN GREEN DRIVE
SUITE 100
RESTON, VA 20190

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-29 are presented for examination.

SPECIFICATION

2.   The objection to the abstract of the disclosure is ***withdrawn*** due to the amendment.

3.   The specification has not been checked to the extent necessary to determine the presence

of all possible minor errors. Applicant's cooperation is requested in correcting any errors of

which applicant may become aware in the specification.

CLAIM OBJECTIONS

4.   The objection to the claims for being incorrectly numbered is ***withdrawn*** due to the

renumbering of the claims.

35 USC § 102

5.   The rejection of claims 1-29 as being anticipated by Moritz is ***maintained*** and updated to

include the amendment to the claims as given below.

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United
> States before the invention thereof by the applicant for patent, or on an international application by another who
> has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention
> thereof by the applicant for patent.

7.   Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Moritz.

8.   Moritz teaches the invention (claim 1) as claimed including a cache memory comprising:

a cache buffer containing most recently accessed data as a multi-bank structure as a cache memory having multiple ways with the ways being equivalent to banks with Tag-Cache being a buffer structure which stores cache line addresses for the most recently accessed cache lines (e.g., see Figure 4, element 210 and paragraph 0105);

a storage array comprising a plurality of cache memory locations and selectively receiving data from the cache buffer which was stored in the memory locations (e.g., see paragraphs 0105 to 0109); and,

a tag memory storing tags associated with data in the storage array and selected data in the cache buffer (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 2, Moritz teaches the cache input data selectively includes executable commands as the cache banks storing instructions executable by the processor (e.g., see paragraphs 0038-0039).

As to claim 3, Moritz teaches a cache input buffer receiving cache input data (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 4, Moritz teaches an output buffer containing most recently accessed data, ones of the tags in the tag memory associated with the most recently accessed data as a CAM based Tag-Cache (e.g., see paragraph 0105).

As to claim 5, Moritz teaches the tag memory comprises a first content addressable memory (CAM) containing tags associated with data stored in the storage array as element 208 and a second CAM containing tags associated with the most recently accessed data with a tag structure being selectively used for most recently accessed cache line addresses as element 210 (e.g., see Figure 4 and paragraph 0105).

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As to claim 6, Moritz teaches a tag for requested data is checked against tags in the

second CAM and the cache input buffer before checking tags in the first CAM as the lookup

mechanism involving Tag-Cache misses (e.g., see Figure 4 and paragraphs 0100 to 0109).

As to claim 7, Moritz teaches each of the first CAM and second CAM are a circulating

first-in-first-out register (FIFO) (e.g., see paragraph 0129).

As to claim 8, Moritz teaches each storage array is a static random access array (SRAM)

(e.g., see paragraph 0074).

As to claim 9, Moritz teaches cache power is substantially less for accessing the data in

the cache buffer than for accessing data in the storage array (e.g., see paragraph 0038).

9.   Moritz teaches the invention (claim 10) as claimed including a content addressable

memory (CAM) random access memory (RAM) cache comprising a plurality of CAMRAM

banks, each of the CAMRAM banks comprising:

a cache buffer containing most recently accessed data as a multi-bank structure as a cache

memory having multiple ways with the ways being equivalent to banks with Tag-Cache being a

buffer structure which stores cache line addresses for the most recently accessed cache line

receiving cache input data, the cache input data selectively including executable commands (e.g.,

see paragraphs 0038-0039 and Figure 4, element 210 and paragraph 0105);

a bank store comprising a plurality of cache memory locations and selectively receiving

data from the cache buffer, selectively received the data being stored in ones of the memory

locations (e.g., see paragraphs 0105 to 0109); and,

a CAM storing tags associated with data in the storage array and selected data in the

cache buffer (e.g., see Figure 4 and paragraphs 0105 to 0109).

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As to claim 11, Moritz teaches the cache buffer comprises an input buffer line receiving a cache input data line and an output buffer containing most recently accessed data, ones of the tags in the CAM being associated with the most recently accessed data with a tag structure being selectively used for most recently accessed cache line addresses (e.g., see paragraph 0105).

As to claim 12, Moritz teaches a cache storage buffer with each input buffer line in the plurality of CAMRAM banks being a line in the cache storage buffer (e.g., see Figure 4).

As to claim 13, Moritz teaches an n-CAM having n tag locations, each n-CAM tag location being associated with one of n storage locations in the bank store and an i-CAM containing i tag locations, wherein $n>i$ and each i-CAM tag location is associated with a location in the output buffer (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 14, Moritz teaches a means for checking a tag for requested data against tags in the i CAM and the cache input buffer independent of tags in the n CAM (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 15, Moritz teaches a checking means only checks for the tag in the n CAM, when the tag is not found in the I CAM or in the cache input buffer (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 16, Moritz teaches cache power is substantially less for accessing the data in the cache buffer than for accessing data in the bank store (e.g., see paragraph 0038).

As to claim 17, Moritz teaches each of the n-CAM and the I-CAM are a circulating first-in-first-out register (FIFO) (e.g., see paragraph 0129).

As to claim 18, Moritz teaches the bank store is a static random access (SRAM) array (e.g., see paragraph 0074).

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10.   Moritz teaches the invention (claim 19) as claimed including a method of managing data

in a cache, the method comprising the steps of:

a) providing incoming data to an input buffer (e.g., see Figure 4 and paragraphs 0105 to

0109);

b) selectively loading data from the input buffer into a storage array (e.g., see Figure 4

and paragraphs 0105 to 0109);

c) selectively loading accessed data from the storage array to an output buffer, a number

of most recently accessed data blocks being held in the output buffer (e.g., see Figure 4 and

paragraphs 0105 to 0109); and,

d) selectively providing data from each of the input buffer, the storage array and the

output buffer responsive to an access request (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 20, Moritz teaches (e) receiving an access request for data and (f) checking

the input data buffer for data requested for access (e.g., see Figure 4 and paragraphs 0105 to

0109).

As to claim 21, Moritz teaches the access request is a store request and the method

further comprising (g) storing the data in the input buffer and (h) marking the stored data as dirty

as updating the Tag-Cache (e.g., see paragraphs 0116-0120).

As to claim 22, Moritz teaches (g) checking the output buffer for the data requested for

access (e.g., see Figure 4 and paragraphs 0105 to 0109).

As to claim 23, Moritz teaches the access request is a store request and the method

further comprising (h) storing the data in the output buffer and (i) marking the stored data as

dirty as updating the Tag-Cache (e.g., see paragraphs 0116-0120).

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As to claim 24, Moritz teaches the output buffer is checked in step (g) coincident with checking the input buffer in step (f) as part of the speculative alias analysis using hotline registers (e.g., see paragraphs 0110 –0122).

As to claim 25, Moritz teaches the data requested for access is not found in the output buffer or the input buffer, the method further comprises the step of (h) checking the storage array for the data requested for access as part of the speculative alias analysis using hotline registers (e.g., see paragraphs 0110 –0122).

As to claim 26, Moritz teaches the data requested for access is found in the storage array, the method further comprises the steps of (i) loading the data requested for access into the output buffer and (j) providing the data requested for access as an output as part of the speculative alias analysis using hotline registers (e.g., see paragraphs 0110 –0122).

As to claim 27, Moritz teaches the data requested for access is not found in the storage array, the method further comprises the steps of (i) sending a miss request, (j) loading the input buffer and (k) providing the data from the input buffer as an output as part of the speculative alias analysis using hotline registers (e.g., see paragraphs 0110 –0122).

As to claim 28, Moritz teaches the input buffer contains data other than the data requested for access, the sending step (h) further comprises loading the other data from input buffer to the output buffer as part of the speculative alias analysis using hotline registers (e.g., see paragraphs 0110 –0122).

As to claim 29, Moritz teaches the data in each of the input buffer, the storage array and the output buffer are identified by tags, the tags being checked in checking steps (f), (g) and (h) as part of the speculative alias analysis using hotline registers (e.g., see paragraphs 0110 –0122).

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RESPONSE TO APPLICANT'S REMARKS

11.   Applicant's arguments filed March 29, 2006 have been fully considered but they are not

persuasive.

12.   As to the storage arrays not being buffered, before or after the array, the cache array is

the buffer. Applicant appears to be misusing this terminology. The claim language does not

require a separate buffer from the cache itself. The cache inputs lines of data when required by

the functioning of the system and outputs cache lines as well. Without further specifics in the

claims, these elements are taught to the extent required by the actual claim language.

13.   As to the storage arrays not communicating with one another, this is not a claim

limitation.

OFFICE ACTION FINALITY

14.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing

date of this final action.

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CONCLUSION

15.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The

examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor

for AU 2187, Donald Sparks, can be reached for general questions concerning this application at

(571) 272-4201. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187

Monday, June 12, 2006

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